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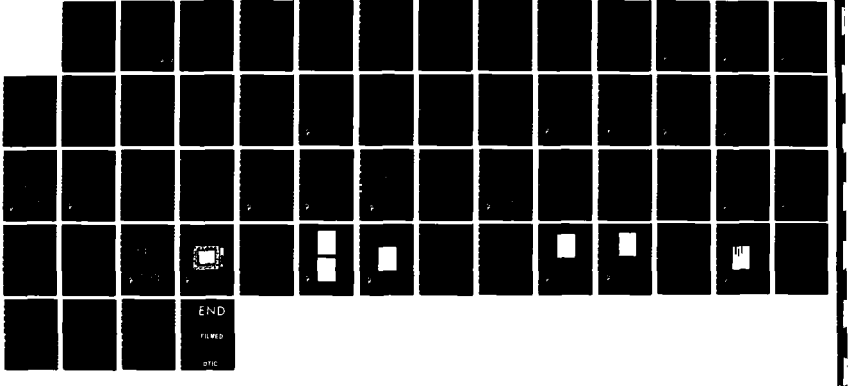

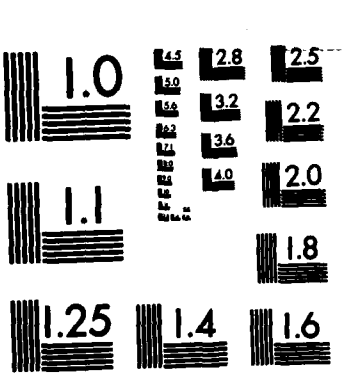

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INVESTIGATION OF HIGH SPEED ICs IN InP USING MIS STRUCTURES

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A 3x3 digital multiplier IC has been developed using InP MISFET technology. A modified enhancement/depletion circuit approach with source follower input transistors was selected for use on the basis of being tolerant to process variations. In a self test mode of the multiplier, multiply times of 11 ns were observed.	

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PREFACE

The work reported here was supported by the Naval Ocean Systems Center, San Diego, California, under N66001-82-C-0290. The program objective was to design, fabricate, and evaluate a 3x3 multiplier using InP as a substrate for high speed circuit integration using MIS structures.

This work was performed by Lockheed Missiles & Space Co, Sunnyvale, CA 94088-3504 and by NOSC in San Diego, CA. Contributions to this work were made by D.K. Kinell, W. F. Parsons, J. M. Stephens, and E. C. Cabudoy at LMSC and M. Taylor, D. Collins, and C. Zeisse at NOSC.

This is the final report which covers the period from 15 October 1982 through 15 June 1984. The submittal date of this report was October 1984.

SECTION II

INTRODUCTION

The evolving requirements on electronic systems which are to operate at frequencies in the gigahertz range are driving the integrated circuit technologies in the direction of new semiconductor materials, such as indium phosphide and gallium arsenide. Such high frequency operation, which is unavailable with commercial silicon circuits, is required for both multigigabit data processing as well as for high speed communications and surveillance applications involving high speed electro-optic circuity.

One of the possible technological approaches to meeting these high speed requirements is to use InP which, like GaAs, has a high saturated electron velocity. In addition InP, unlike GaAs, also appears to possess favorable surface properites allowing the formation of MIS structures similar to NMOS devices in silicon technology. Furthermore InP MIS transistors can be fabricated as either normally-off enhancement (or accumulation mode) devices or as the more common depletion type device. What this means is that InP may well be the choice where high speed, low power, and simple circuit design are most important.

Enhancement (or accumulation) mode devices permit the design of direct coupled logic without the need for additional circuitry to perform level shifting. This simplicity of design results in fewer transistors as well as less area required for a particular integrated circuit layout. These effects are expected to result in higher circuit yield and higher reliability with the added benefit of a reduction in power consumption.

Enhancement (or accumulation) mode devices permit the design of direct coupled logic without the need for additional circuitry to perform level shifting. This simplicity of design results in fewer transistors as well as less area required for a particular integrated circuit layout. These effects are expected to result in higher circuit yield and higher reliability with the added benefit of a reduction in power consumption.

Another advantage of InP MIS direct coupled logic over MESFET or JFET type circuits is the improved noise immunities made possible with insulated gate structures. In the InP MIS device, forward gate voltages are not restricted by the limited current capacity of small Schottky or PN junction gates operating in the forward bias region. In the MIS gate, several volts of logic swing are possible whereas in the MESFET or JFET cases, gate conduction with an applied positive voltage limits the logic voltage swing to typically less than one volt.

The objective of this program is to exploit the advantages of InP MIS technology by way of an MSI level logic circuit incorporating about 75 to 100 logic gates. Such a circuit is a high speed digital multiplier which not only provides a vehicle for a technology demonstration but also is a useful design with practical applications. The digital multiplier is an important building block in performing fast fourier transforms (FFTs) as well as other signal processing applications. Speed comparisons with other technologies are easily made as the time delay of a given multiplication is determined by the choice of architecture and fabrication technology.

SECTION III

MULTIPLIER ARCHITECTURE

This 3x3 digital multiplier utilizes combinational logic operating on two 3 bit binary numbers and through a series of binary multiplications and additions a 6 bit binary product is provided. The block diagram of the 3x3 digital multiplier, as shown in Figure 1, reveals the flow paths for obtaining the required product. The least significant product bit, called Po, is the product of the least significant input bits, Xo and Yo. Subsequent product bits require increasingly more complex logic with the most complex path being for the last or most significant product bit, P5. The data path for P5 requires several summing and carrying additions as well as multiplications of input bits before an output is achieved. When examing the time required for a multiplication the least significant bit arrives at the output in the shortest time, with the most significant bit requiring a period determined by the number of multiplications, additions and carries in its path. Thus as the number of multiplier input bits increases, longer multiplication times occur before the most significant product bit is valid.

In the 3x3 multiplication process, each logic bit of the input multiplicand is multiplied by the logic bit of the multiplier, such as Xo times Yo as mentioned above. In binary arithmetic multiplcation is equivalent to the AND function, or if the logic complement is used (inputs inverted), then a NOR gate performs this operation. For a 3 bit multiplication process nine of these gates are required as depicted in Figure 2 which shows the overall logic diagram of the 3x3 multiplier. Here, inverted inputs are created by the input buffers of the multiplier (not shown) with a total of 9 NOR gates required in this design for establishing all

the initial multiplier products. Except for the least significant product, Po, all products require routing of signals through some combination of adder circuits. If addition requires a carry input a full adder, (F.A.), circuit is used whereas if no carry input is required only a half adder, (H.A.), is required. In either case the adders have two outputs, one called Sum and the other Carry, with signal routing depending on the particular logic path required by the multiplier algorithm. For the most significant bit the logic path requires up to four carry additions before the signal is obtained at the P5 output.

In order to use the 3x3 multiplier as a practical demonstration circuit one additional feature to the basic design provides a convenient method to evaluate circuit operational speed. This design includes a self test mode in which the multiplier operateds in an oscillatory or ring oscillator mode. As shown in the complete multiplier block diagram of Figure 3, the addition of a few extra logic gates allows this self test mode to be available.

In operation, once the self test mode is enabled, a logic one is applied to all the Y inputs and also to the most significant bit of the X inputs. The XO bit is maintained at logic zero. For oscillation to occur the most significant output bit, P5, is inverted and provided as an input bit to the least significant X inputs. The equation becomes:

$$
\begin{array}{rcccl}
 & 1 & 1 & 1 & = Y \\
\times & 1 & 0 & P5 & = X \\
\hline
 & \overline{P5} & \overline{P5} & \overline{P5} & \\
1 & 1 & 1 & 0 & \\
\hline
\overline{P5} & P5 & P5 & P5 & \overline{P5} \quad \overline{P5}
\end{array}
$$

Figure 1

3x3 DIGITAL MULTIPLICATION

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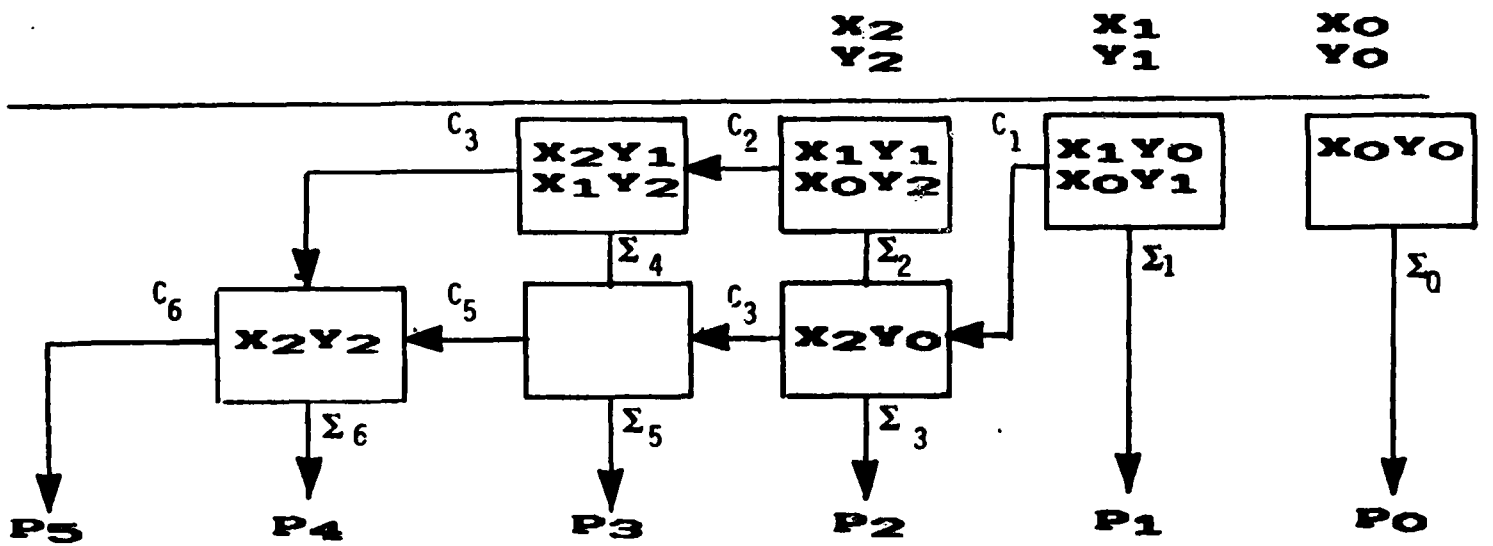

Figure 2

LOGIC DIAGRAM - 3X3 MULTIPLIER

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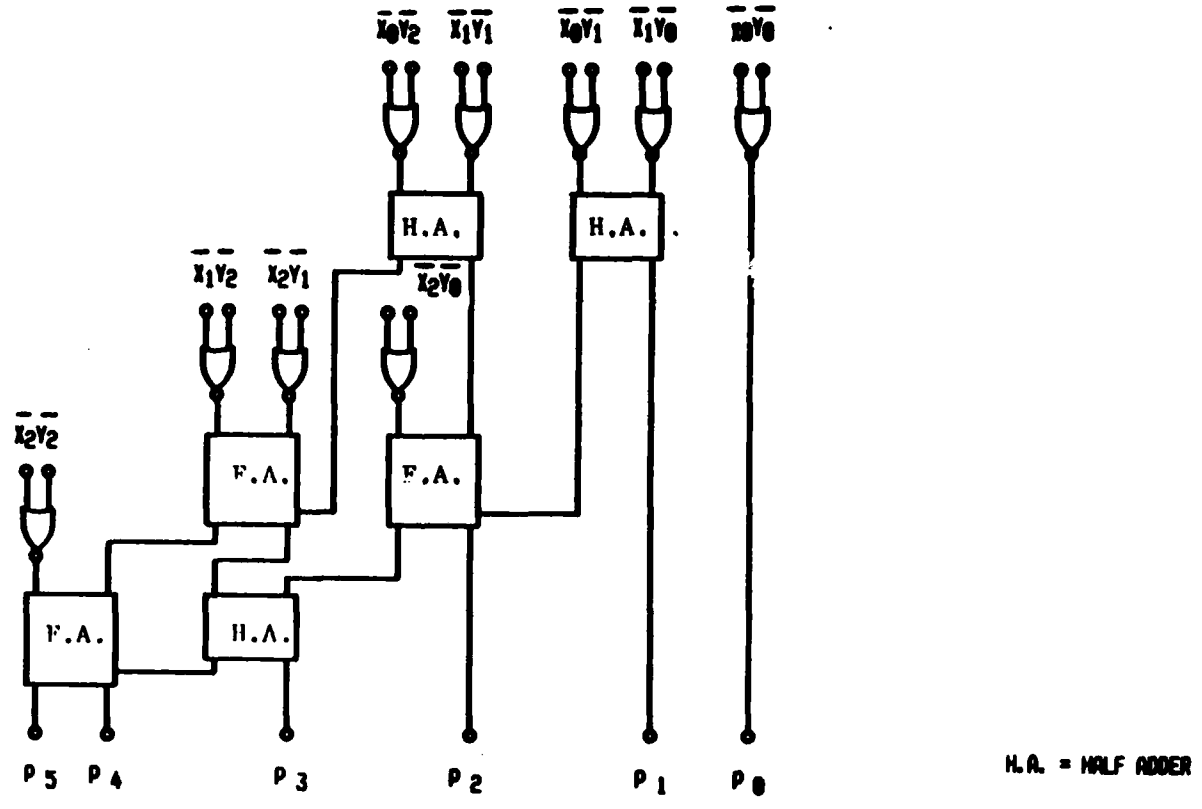

Figure 3

BLOCK DIAGRAM - 3X3 MULTIPLIER

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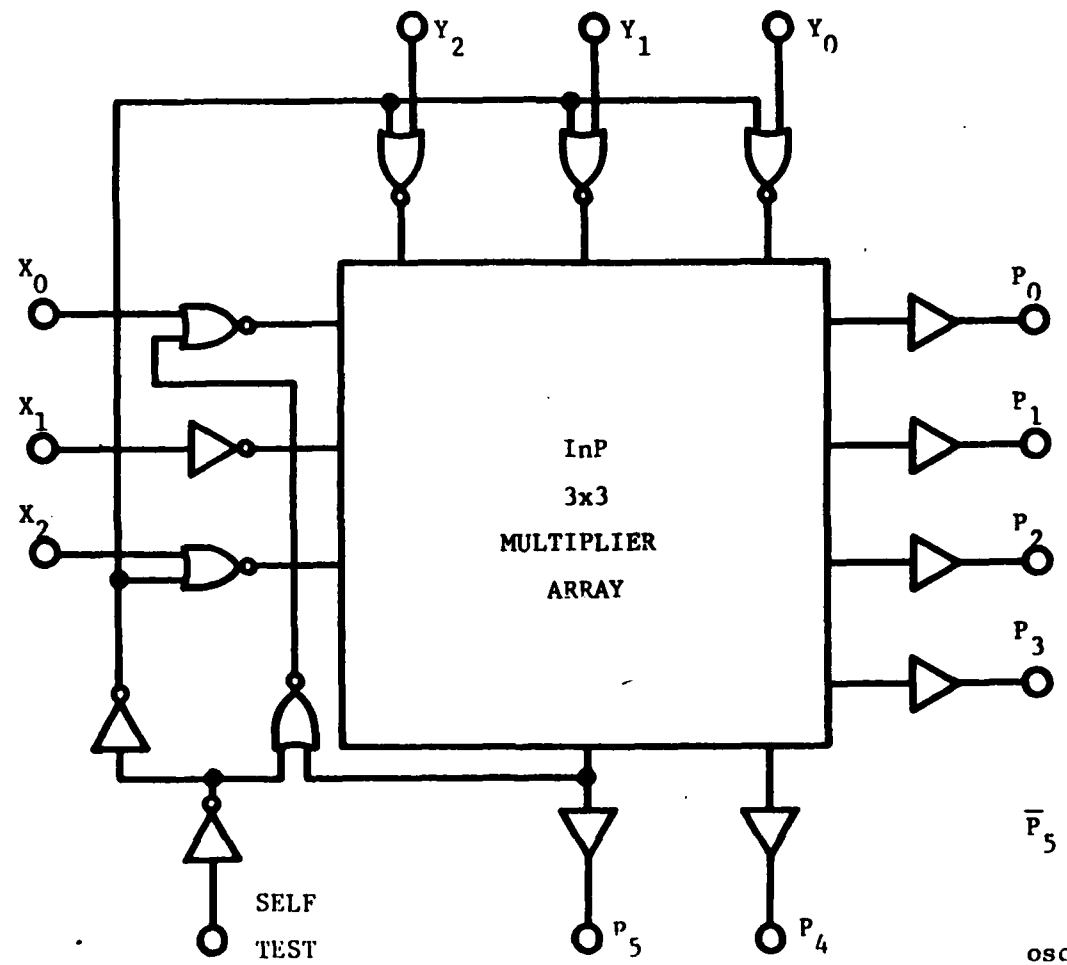

FOR SELF TEST

1 1 1 = Y

x 1 0 $\overline{P}_5$ = X

$\overline{P}_5$ $\overline{P}_5$ $\overline{P}_5$

1 1 1 0

$\overline{P}_5$ P_5 P_5 P_5 $\overline{P}_5$ $\overline{P}_5$

P_5 becomes $\overline{P}_5$

oscillates at 1/9 T_d

where P5 changes to $\overline{P5}$ after one cycle of the multiplication operation. This condition forces the unit to oscillate. For this particular 3x3 multiplier architecture and circuit design the period of oscillation is nine times the time delay of the basic logic gate and therefore from the oscillation frequency of the multiplier, individual delay times of the logic gates can be found.

The choice of a 3x3 digital multiplier for demonstration of the InP MISFET technolgy provides MSI levels of circuit integration as well as a self test mode of circuit operation for gate delay measurements. These performance numbers provide accurate gate delay times as realistic fanout and capacitive loading of interconnects are included in this measurement.

SECTION IV

LOGIC GATE OPTIONS

Logic gate design is a key element for success in that optimum operation of the multiplier adders, half adders and other logic gates depend upon a combination of good noise immunity, maximum switching speed, and minimum power dissipation. For a logic gate to function properly it must be able to interpret its input voltages as to either a logic 1 or else a logic 0. An inverter in which the transistion state is only a few tenths of a volt away from either the high or low values may fail to operate over worst case device variations of threshold voltage and current gains. Thus the circuit design choice of a logic inverter needs to consider these process variations in order to guarantee circuit operation.

The switching delay of an inverter is determined by a combination of transistor current gains and circuit capacitances. An advantage of InP MISFET circuits over silicon designs is the improved current gains made possible by the high electron velocities inherent in the InP material. This results in transistors which provide high currents in a short time for charging capacitive loads. Thus circuit switching times are decreased for equivalent InP designs. Even with basic material advantages, optimization of logic delay times are possible with different circuit designs in which input capacitances are minimized and output drive currents are maximized.

A final consideration for logic gate design is power dissipation which is determined by the particular circuit design of the logic gate as well as the specific geometric ratios for the transistors. Circuit operating power is minimized by selecting small transistor sizes. However as geometries are minimized, the ability to charge integrated circuit interconnect capacitances is reduced. Therefore optimum circuit performance is a tradeoff between allowable power dissipation and transistor sizes required for highest switching speeds.

For the basic logic inverter structure to be used in the InP multiplier three different candidates were considered. They are:

(1) Simple enhancement-depletion inverters,
(2) Buffered output enhancement-depletion inverter
(3) Buffered input enhancement-depletion inverter

Each of these designs, as shown schematically in Figure 4, were analyzed using a modified SPICE circuit analysis program. Calculations were made on the speed performance and noise immunities for each of the three inverters with various variables being threshold voltage and power supply voltage. The three candidates and their strong and weak points are as follows:

1. SIMPLE ENHANCEMENT-DEPLETION INVERTER

This inverter, as shown in Figure 4a, is the simplest of the three candidates in terms of transistor count with only two transistors required for the logic function of inversion. Furthermore integrated circuit layout is simplified when only two transitors are required per inverter. When compared to the other two potential choices this inverter operates at lower power supply voltages and also lower power levels due to the lower transistor count. If transistor threshold voltages were controllable to a high degree of predictability this design would be an ideal choice. In practical InP MIS circuits the threshold voltage can very significantly from wafer to wafer and across each wafer and as the threshold voltage of the enhancement (or accumulation mode) device approaches zero, noise immunity becomes a real problem in that the inverter cannot be completely turned off. This results in low output voltages over most of the range of input voltages. In terms of geometric layout affecting noise margins, gate widths of the enhancement transistor is typically made several times that of the depletion device. This increase in size for the input transistors causes the corresponding input capacitance to be

relatively large. What this means for this inverter design is a sacrifice in speed of operation in order to obtain needed noise margins.

2. BUFFERED OUTPUT ENHANCEMENT DEPLETION INVERTER

This inverter, as shown in Figure 4b, adds a source follower and pulldown transistor to the inverter of Figure 4a. The addition of the source follower transistor means that higher current drive is possible than with the former case for similar size input devices. This is possible as the source follower transistor gate to source voltage can be forward biased whereas the gate to source voltage is fixed at zero volts for the simple inverter design. Therefore this logic gate is ideal for driving large capacitive loads and will operate faster for large fanouts than the simple E/D gate. This inverter also offers improved noise immunity over the previous design in that geometric scaling of the various transistors is possible in such a way as to partially offset the effects of enhancement transistors with threshold voltages near zero. These improved characteristics of improved current drive and noise immunity are achieved at the expense of increased current drain due to the two current legs of this inverter type. Furthermore, when this gate is expanded to a three input NOR gate configuration, much of the improved noise immunity is lost as this design requires additional enhancement transistors on the inputs. This effect will be discussed further in a following section of this report. The source follower output also has a limited voltage swing due to the voltage drop required from gate to source to maintain this transistor in a conductive state. Furthermore, the power supply voltages for this inverter will need to be higher than the simpler case as the source follower circuit operates best at higher voltages. These combined effects result in higher operating powers than the simple E/D circuit, but when considering functionality of the circuit over worst case conditions, this more complex design is an improvement one over the simpler design described above.

3. BUFFERED INPUT ENHANCEMENT DEPLETION INVERTER

By a slight rearrangement of the previous inverter structure of Figure 4b, another inverter is possible. This inverter, as shown in Figure 4c, uses a source follower and a current source pulldown as the input circuit. For the output circuit an enhancement depletion combination like that of Figure 4a is used. This combination offers improved noise immunities over the first two inverter circuits when the dimensions of the four transistors are optimized. The source follower input transistor results in a low input capacitance and this translates to good circuit speed performance. The output circuitry can swing the full range of supply voltage without adding the voltage drop of the source follower circuit as in the case above. When complex logic functions are used, such as OR-NAND gates, this gate is easily expandable to implement these functions with minimum increases in circuit area. For such implementations the pulldown transistor will need optimization in size, depending upon the total number of input transistors. As in the previous case, two additional transistors are required to implement this gate, which also means increased power dissipation for this gate configuration as compared to the simplest gate design. Furthermore higher supply voltages are required to operate this gate due to the internal source follower transistor but this increase is a small sacrifice to guarantee circuit operation under worst case threshold voltage situations.

Figure 4

INP MISFET INVERTER OPTIONS

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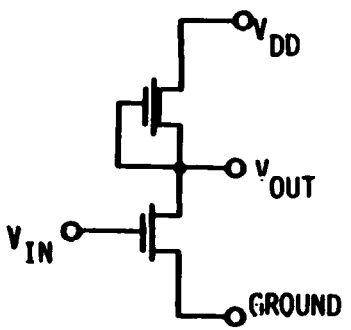
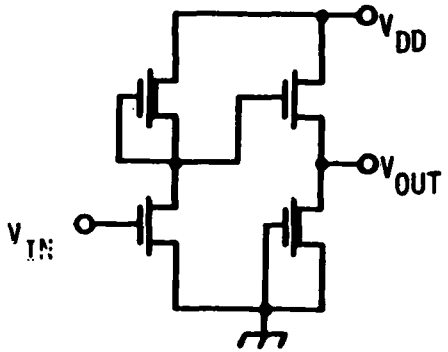
Figure 4a



ADVANTAGES
- Low Transistor Count
- Simple Layout
- Low Voltage Operation
- Low Power

DISADVANTAGES
- Poor Noise Immunity
- Slower Speed
- Large Transistor Sizes
- Large Input Capacitance
- Will Not Operate For Low V_t Of Enhancement Device

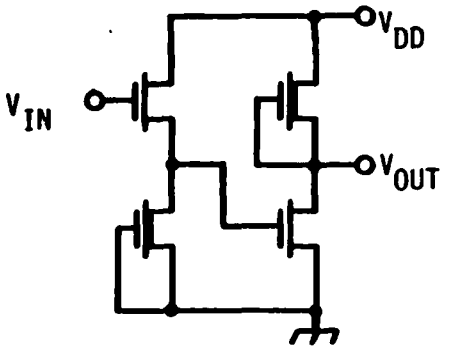
Figure 4b



ADVANTAGES
- Better Noise Immunity Than E/D
- Higher Speed Than E/D
- Small Layout For Complex Logic Gates

DISADVANTAGES
- Higher Power Than E/D
- Larger Transistor Count
- May Not Function For 3-Input NOR Gates With Low V_t
- Low Voltage Swing
- May Not Operate at Low V_{DD}

Figure 4c



ADVANTAGES
- Best Noise Immunity
- Higher Speed Than E/D
- Low Input Capacitance
- Smallest Layout Size For Complex Logic Gates
- High Logic Voltage Swing

DISADVANTAGES
- Higher Power Than E/D
- Larger Transistor Count
- Limited V_{DD} Range
- Pull Down Transistor Size Needs Optimizing For Logic Functions

SECTION V

COMPUTER MODELLING AND LOGIC GATE CHOICE

The design of the various circuits for the InP 3x3 Multiplier involved computer analysis to determine the best geometric ratios in order to achieve optimum multiplier performance. The starting basis for any circuit analysis is the model used for the active transistors, in this case both depletion and enhancement (or accumulation) MIS type transistors. The approach taken here was to establish a computer model based upon actual (not theoretical) device characteristics. This way the relative performace of each of the InP MISFET circuits will realistically be simulated.

Many computer analysis programs are available with easy access and use, particularly on a timeshare type computer terminal. In particular Lockheed utilizes ISPICE, provided by NCSS, Inc. and supported by Electrical Engineering Software, Inc. for simulating performance of integrated circuit designs. This program provides good flexibility in generating device models in that circuit equations are programmable by user defined variables such as doping levels, oxide capacitance, mobility, transconductance, and even velocity saturation effects for short channel lengths. The end result is that transistor models can be generated for both DC and transient effects without concern as to which technology the circuit is being fabricated in. Thus this approach is very useful for InP MISFET devices where the availability of computer models is limited.

For InP MISFET technology, the easiest approach for circuit simulation is to modify a silicon MOS model by redefining the parameters to fit the various characteristics of the InP devices. This revised model is then used to design and characterize the circuits needed for the 3x3 multiplier.

One of the device parameters that is important for circuit design is the variation in threshold voltage that is encountered from wafer to wafer. For the purposes of circuit analysis, the depletion device was assumed to have a variation of threshold voltage from -2.2 volts to -3.0 volts. The enhancement device was assumed to vary from -0.5 volts to +0.5 volts and thus was allowed to vary from normally on to normally off as a result of wafer to wafer process variations. The results of this device simulation is plotted in Figure 5 for the depletion devices and Figure 6 for the enhancement transistors. These figures plot the drain current, in milliamps, of a 40 x 1.5 micron transistor versus drain voltage. For the depletion devices of Figure 5, the gate voltage ranges from 0.0 volts (top curves) to - 3.0 volts in 0.5 volt increments with drain voltages extending to 10.0 volts. For the enhancement transistors of Figure 6, the gate voltage ranges from 0.0 volts (bottom curves) to +7.0 volts in 1.0 volt step increments with drain voltages also extending to 10.0 volts. These enhancement and depletion transistor models were then used in all the subsequent design evaluations of the various multiplier circuits.

The first series of circuits to be evaluated were the inverter choices described in Section IV, Logic Gate Options. The primary concern of the final logic gate design was whether logic gate functionality is achieved over all ranges of threshold voltage variations and circuit configurations. A worst case situation occurs for the three input NOR gate in which three enhancement transistors are in parallel at the input to the logic gate. If the turn on voltage of these transistors is slightly below zero volts, current will flow in the logic gate when none is supposed to. This results in a lowering of the output voltage and in the worst case, the output voltage for zero volts input will be lowered by a critical amount, in which case, the following stages of logic gates may fail to operate.

The potential problem of loss of noise immunity was analyzed very carefully for the three inverter choices mentioned previously. The results for the source follower output and source follower input are plotted in Figures 7 and 8 respectively. As shown in Figure 7, a slightly negative enhancement turn on voltage results in a loss of noise immunity for the case of a three input NOR gate, even though the basic inverter structure has acceptable noise margins. However for the source follower input design of Figure 8, adequate noise margins are achieved for the case of three input transistors. The other remaining circuit choice, using the simple two transistor enhancement depletion structure, exhibited characteristics similar to the source follower outut results of Figure 7.

Based on the circuit simulation results, the best approach to guarantee successful operation of the 3x3 InP multiplier is the source follower input configuration of Figure 4c. This logic gate was thus selected as the starting point for all the various circuits required to implement the 3x3 multiplier architecture. The best choice for a highly controllable process would have been to use the simple configuration of Figure 4a, but worst case conditions would have made this choice inoperable.

Figure 5

INP MISFET DEPLETION MODELS

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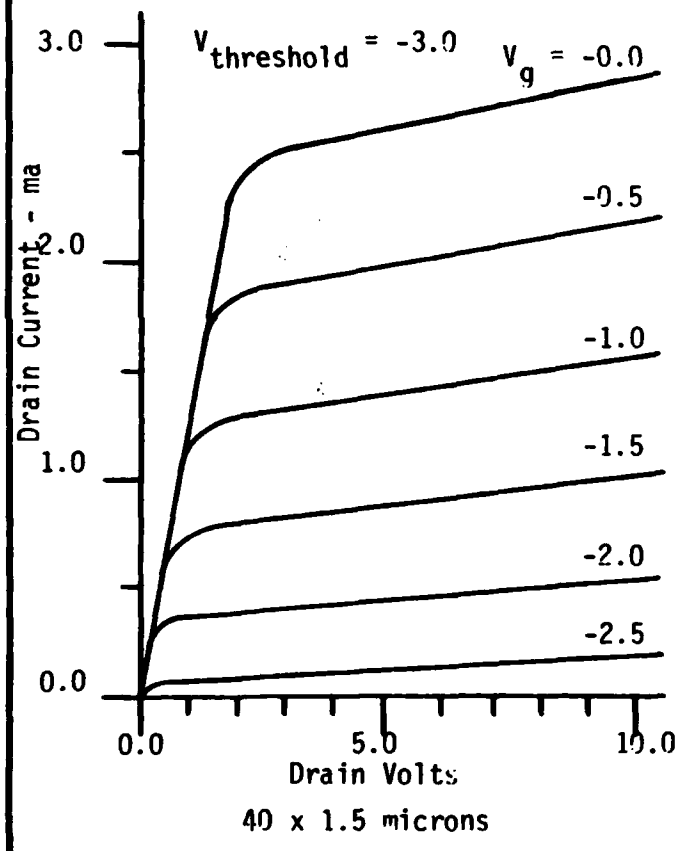

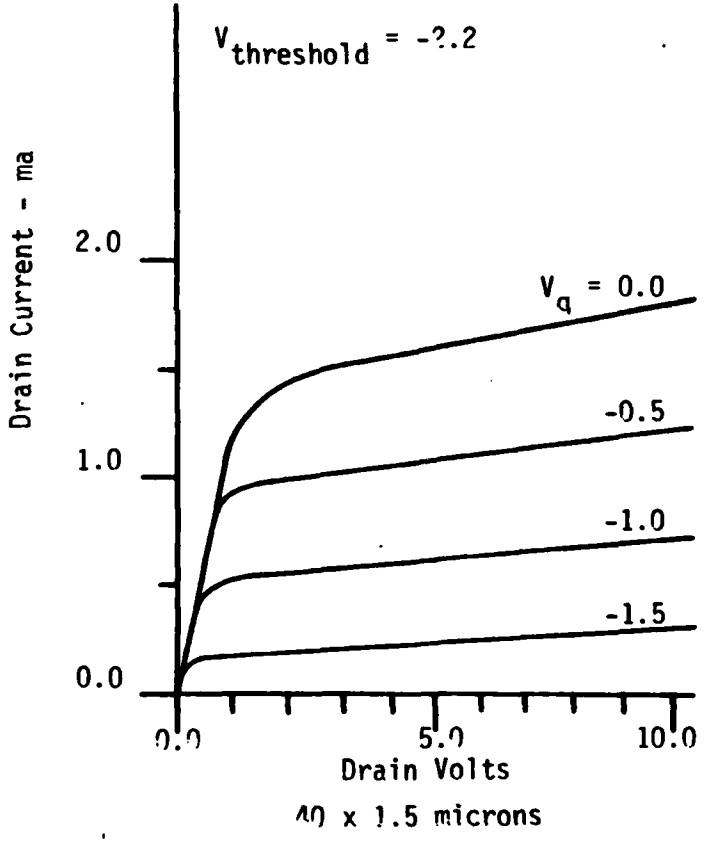

Figure 6

INP MISFET ENHANCEMENT MODELS

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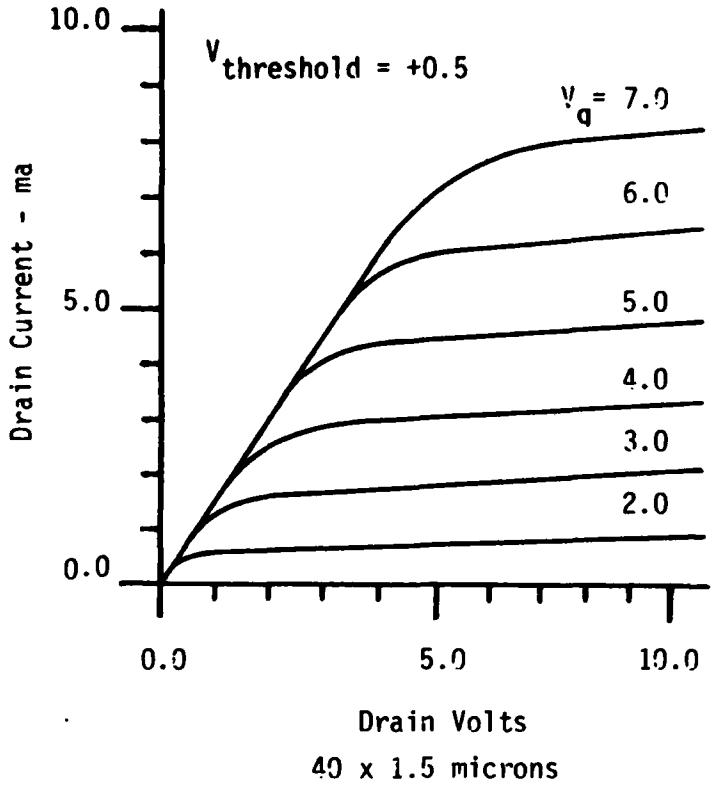

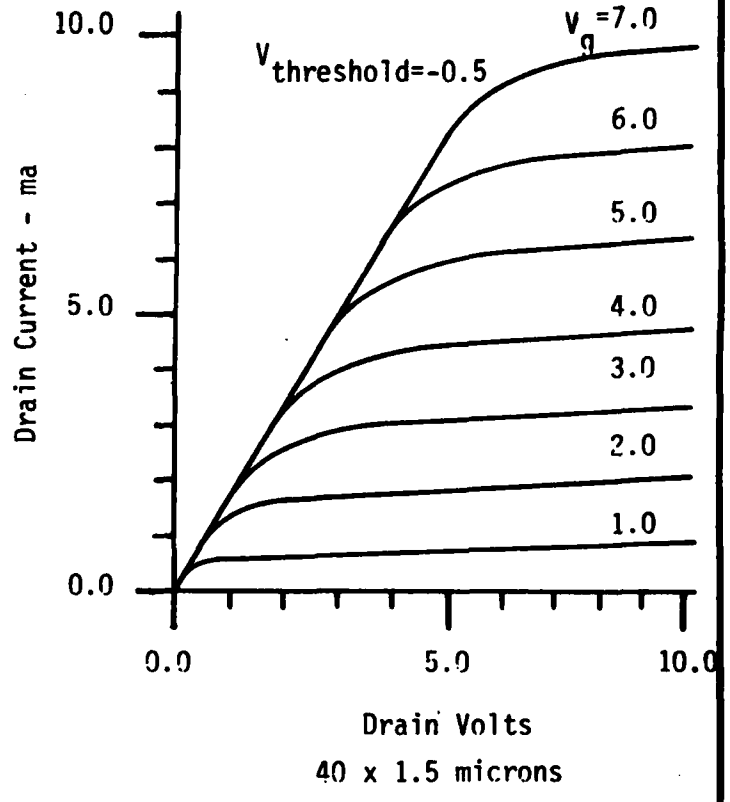

Figure 7 **InP MISFET-WORST CASE SOURCE FOLLOWER OUTPUT**

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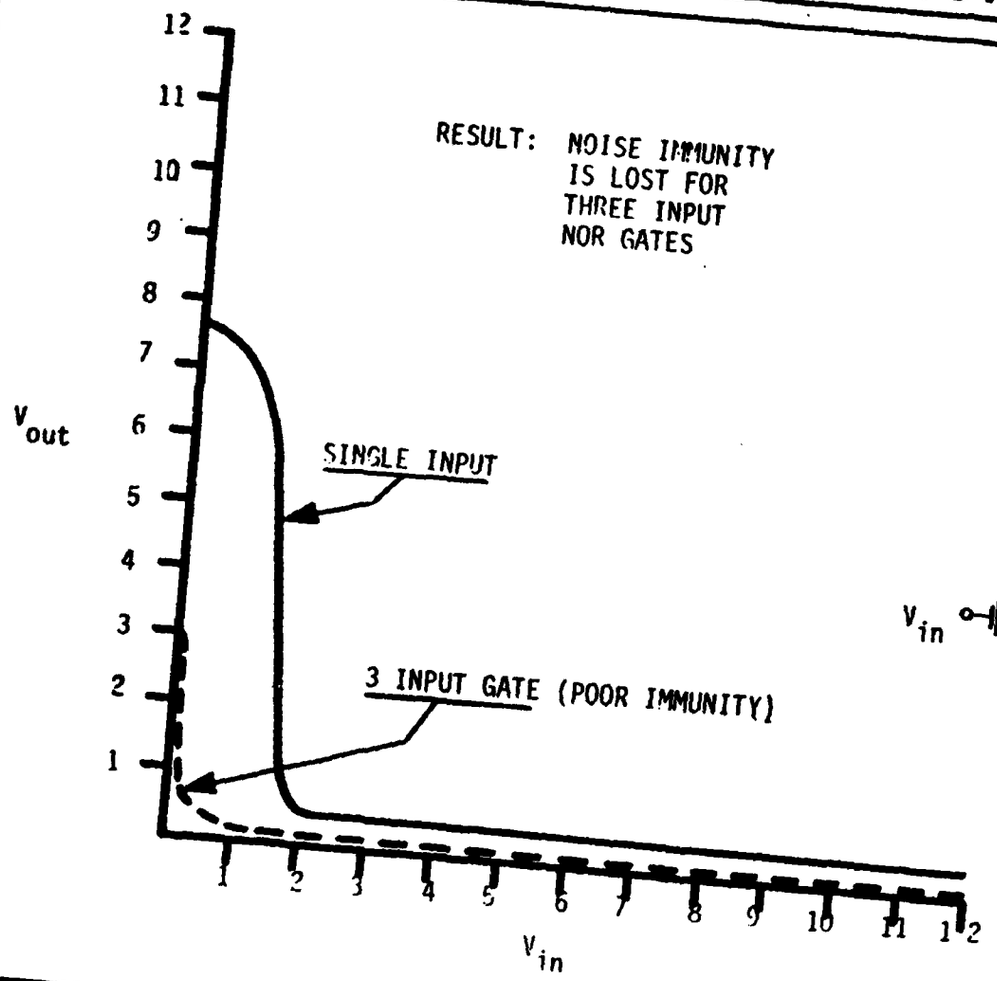
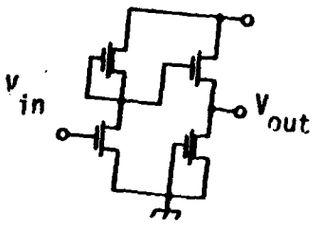
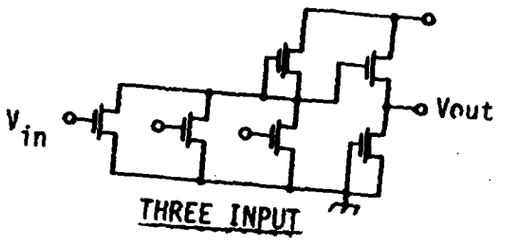


RESULT: NOISE IMMUNITY IS LOST FOR THREE INPUT NOR GATES



SINGLE INPUT



THREE INPUT

ASSUME: V_t = -0.5 Volts
V_{DD} = 12.0 Volts

Figure 8 **InP MISFET-WORST CASE SOURCE FOLLOWER INPUT**

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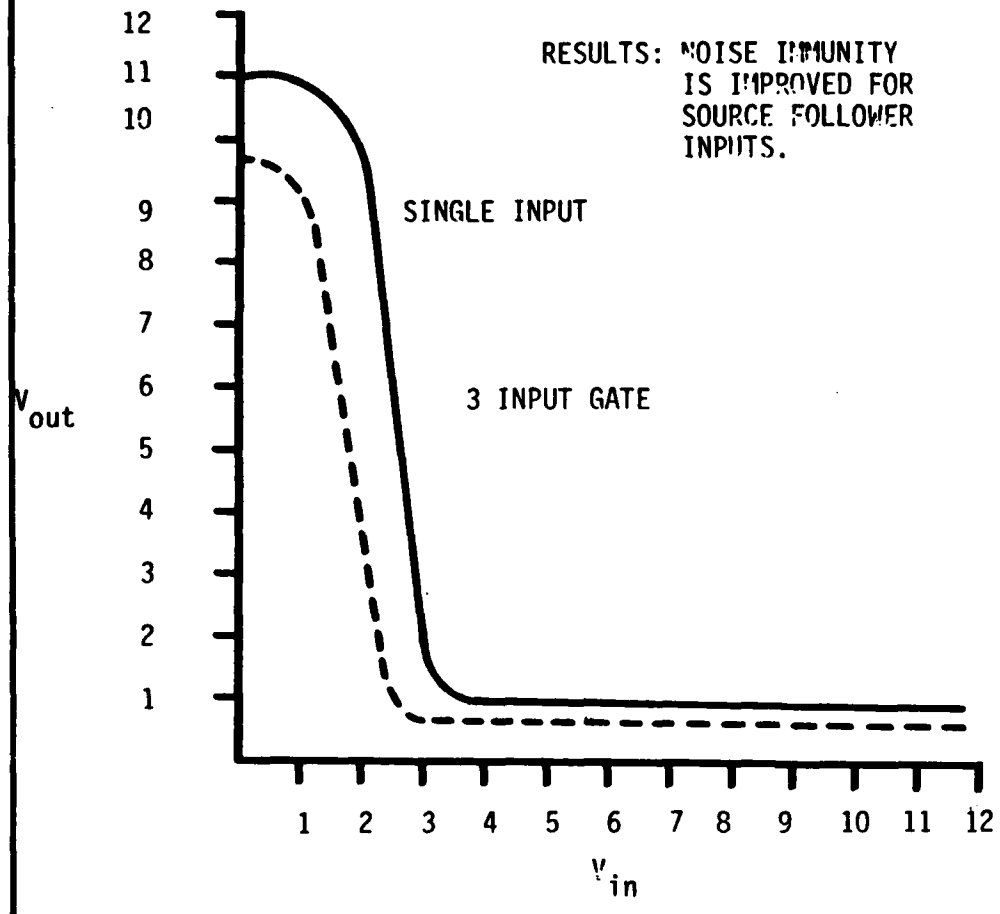
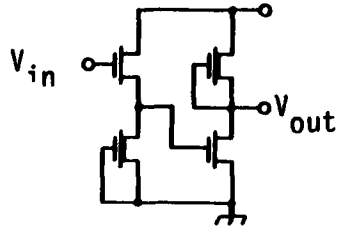
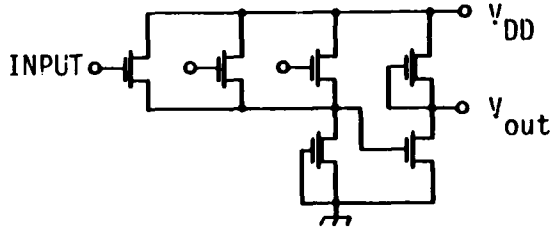


RESULTS: NOISE IMMUNITY IS IMPROVED FOR SOURCE FOLLOWER INPUTS.



Single Input



Three Input

ASSUME: V_t = -0.5 Volts

V_{DD} = 12.0 Volts

SECTION VI
MULTIPLIER LOGIC BLOCKS

The first circuit to be implemented with the source follower input configuration is the OR/NAND gate as shown in Figure 9. By wiring the four input transistors as shown in Figure 9, a complex gate can be created which uses two levels of logic within one circuit instead of the more familiar single level of logic obtained from an inverter. By this approach, logic delay paths are shortened and the total number of transistors is reduced. Referring to Figure 9, the two input NOR function is the combination of one of the two top input transistors or a combination of the lower two parallel transistors. These pairs, by being in series, are logically ANDED, and with an output inverter, a NAND function results. This OR/NAND gate is very useful in the subsequent creation of half and full adder circuits.

A computer analysis of the OR/NAND gate was performed to evaluate its functionality and logic delay times for worst case conditions of threshold voltages and power supply values. As a basic building block for the whole multiplier, the operation of this gate is critical and therefore must function over these worst case conditions. The results of this analysis are tabulated in Figure 10. In order to simulate actual fanout loading of this gate, four additional logic gates were added to the output in order of provide for realistic capacitive loads. The simulation provided for switching the OR/NAND gate under all conditions as shown by the pattern of the input wave forms. This was done to observe the sensitivities to placement of signals on either upper transistor pairs or lower transistor pairs and in fact there is a difference in response times as the table shows. As previously mentioned, the enhancement transistor threshold voltages varied from -0.5 volts to +0.5 volts and the depletion threshold voltages varied from -2.2 volts to -3.0 volts. The analysis was performed at supply voltages of +7.0 volts and +12.0 volts. As indicated on the input and output waveforms, four time delays were calculated, each one for a different variation of input signals.

Figure 9

INP OR/NAND LOGIC GATE

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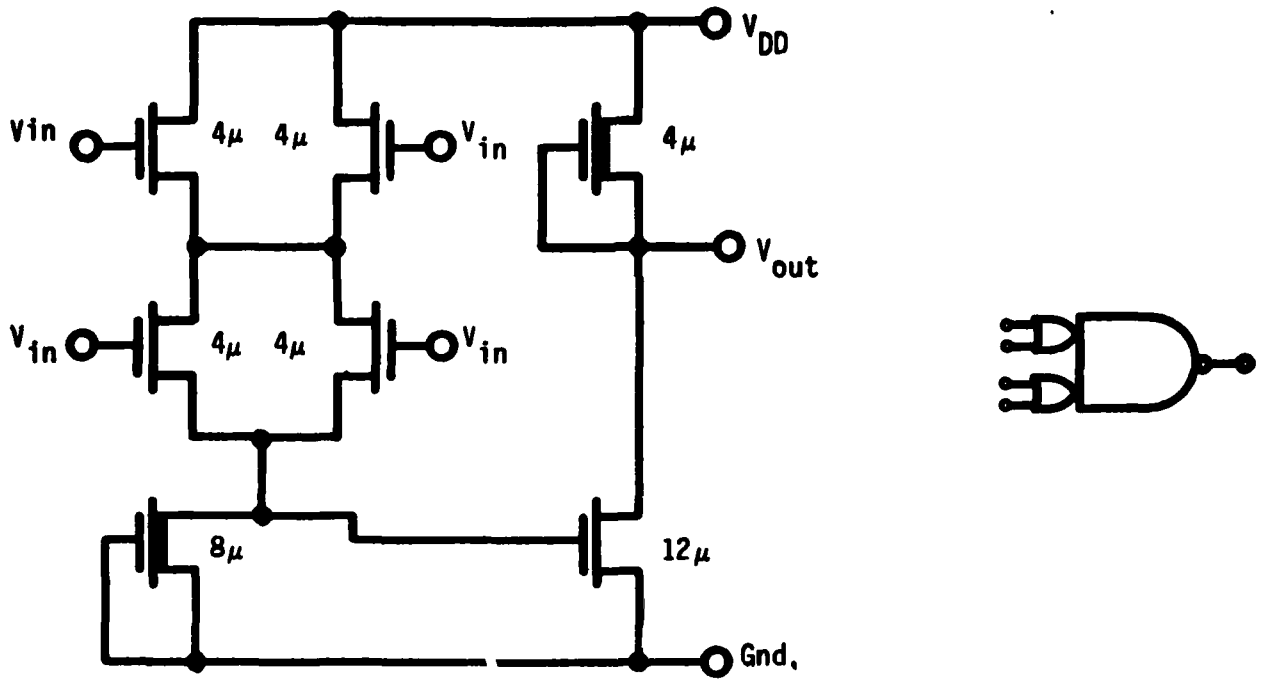

Figure 10

OR/NAND LOGIC GATE ANALYSIS

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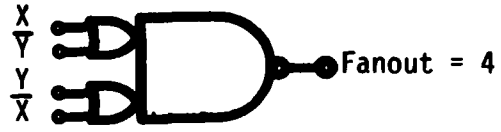

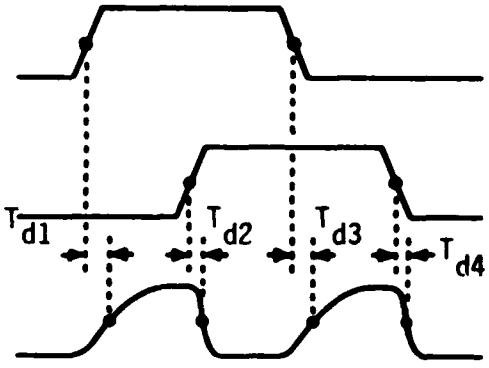

CIRCUIT CONDITIONS	Td_1	Td_2	Td_3	Td_4
Vdd = 12 volts				
Vte = -0.5 volts Vtd = -2.2 volts	600 ps	50 ps	1000 ps	50 ps
Vte = +0.5 volts Vtd = -3.0 volts	350 ps	100 ps	450 ps	300 ps
Vdd = 7.0 volts				
Vte = -0.5 volts Vtd = -3.0 volts	400 ps	100 ps	650 ps	250 ps
Vte = +0.5 volts Vtd = -3.0 volts	Inverter did not function			

The general results are that the fall time delays tend to be short compared to the rise time delays. This is due to the differences in drive currents available between the enhancement and depletion transistors. Another observation is that under some worst case conditions of threshold voltages, coupled with a low power supply, the OR/NAND gate may not function properly. In this case increasing the supply voltage corrects the situation. A considerable variation in propagation delay occurs for placement ofinput signals on the top pair of OR gate transistors and placement of signals on the bottom pair. For example in the case where the supply voltage is 12 volts and the enhancement and depletion threshold voltages are -0.5 volts and -2.2 volts respectively, a time difference of 400 picoseconds occurs. In other words, if a positive signal is applied to one of the top transistors, the delay time is 600 picoseconds but if this same signal is applied instead to one of the bottom pair of transistors, the overall gate delay is increased to 1000 picoseconds. This difference is due to charging current variations between the two cases. The important aspect of this analysis is to apply critical signal paths to the gates with the lowest delay times.

The OR/NAND gate is used to create additional multiplier building blocks. In the implementaion of a half adder circuit, there are several methods that can be used, some of which require fewer logic gate delays than others. For example, the sum output can be available in only one gate delay if the OR/NAND gate configuration of Figure 9 is used. Other methods of half adder implementation require more gates with longer delay paths. Thus for high speed multipliers, the circuit of Figure 11 was selected as the method for finding the sum and carry of two numbers. This half adder, as used in the 3x3 multiplier, requires two OR/NAND gates as well as two simple two input NOR gates. The only requirement for this type of half adder design which is different from other configurations of half adders is that the true and complement of the input logic signals be available for the

addition process. This is easily done by inverting the X and Y input signals at the input stages of the multiplier. Note that the output of the half adder automatically creates true and complemented sum and carry signals which are again used in subsequent stages of the multiplier.

When addition requires a carry input signal as well as the two sum inputs, a full adder configuration is required. Again, by using the basic OR/NAND gate of Figure 9, a minimum delay full adder circuit can be easily implemented. For this case, the requirements are for six of the OR/NAND gates to be used as well as a single inverter as shown in Figure 12. Also shown is a wired OR configuration which is simply the electrical connection of the outputs of two OR/NAND gates. The complemented inputs and outputs result in more logic signals but with a gain in operating speed for the arithmetic process.

Another basic design block of the multiplier is the input buffer which was designed to be compatible with high speed silicon ECL logic signals. Since most compatible test equipment is designed to provide signals with ECL voltage levels, testing of the InP multiplier would be easier if these same signal levels could be used for the InP design. Voltage level shifting between the test instrumentation and the InP multiplier was designed to be on-chip instead of incorporated in special interface circuits. This way potential speed delays that occur between the test equipment and the InP circuit would be minimized. Furthermore as inversion of the input signals was necessary in any case, inclusion of a voltage buffer was easy to implement in the design of the multiplier input buffer which is shown in Figure 13. In fact two transistors accomplish the transistion from the one volt signal levels of ECL logic to the several volt levels of the InP logic. Overall, seven input buffers were used by the multiplier, five of which incorporated an additional transistor in parallel to the second stage input transistor to achieve a NOR function. This additional gating was added to the input buffers for controlling the input signals in the self test mode as shown in Figure 3.

Figure 11

INP HIGH SPEED HALF ADDER

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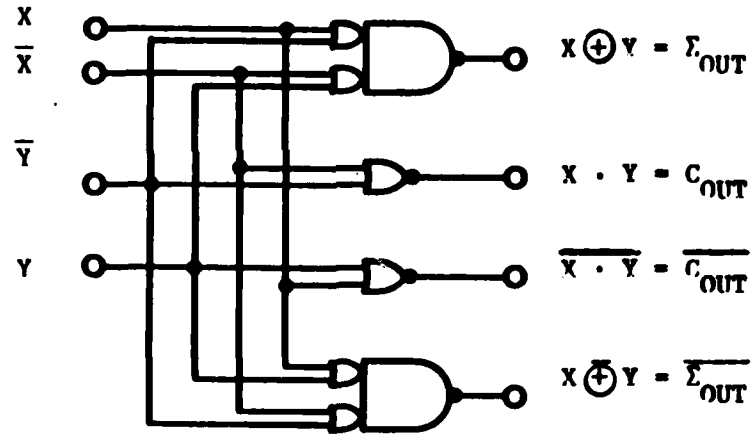

Figure 12

InP HIGH SPEED ADDER

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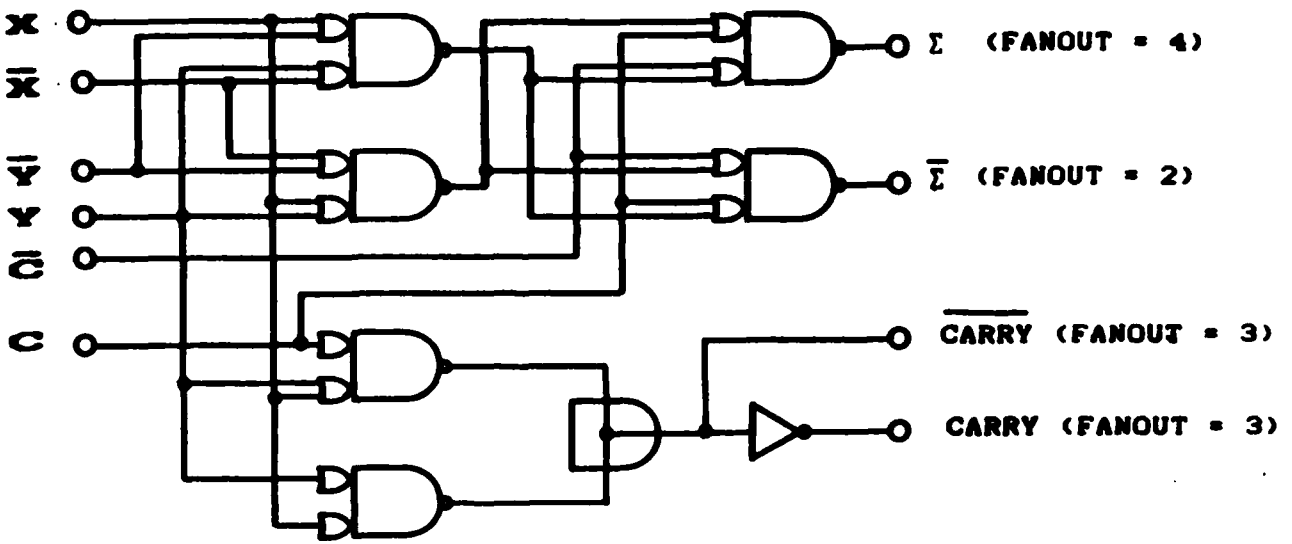
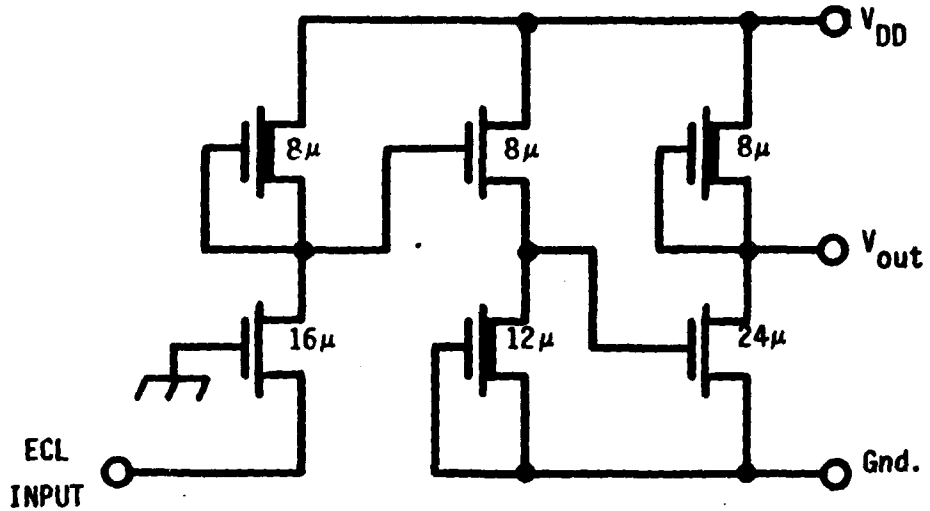


Figure 13 INP ECL COMPATIBLE INPUT BUFFER

microelectronics



A final building block for the InP multiplier is the output driver circuit. Here, the requirement is to receive the product bit signals without adding any significant capacitive loading and be able to drive a 50 ohm load at ECL signal levels. The design shown in Figure 14 meets this requirement. The input transistors to the output buffer are kept relatively small (at 8.0 microns in gate width). This way signals from the various adders are not degraded by a large capacitive load. Two inverter stages amplify the output signal with a source follower being incorporated as the final output drive for 50 ohm loading. Note also the incorporation of a separate power line for the output transistor. This was included in the layout of the multiplier so that output current transients which cause spiking on the power supplies would be isolated from the internal logic. Overall, six output buffers were used in the design of the InP 3x3 multiplier.

Figure 14 InP ECL COMPATIBLE OUTPUT BUFFER

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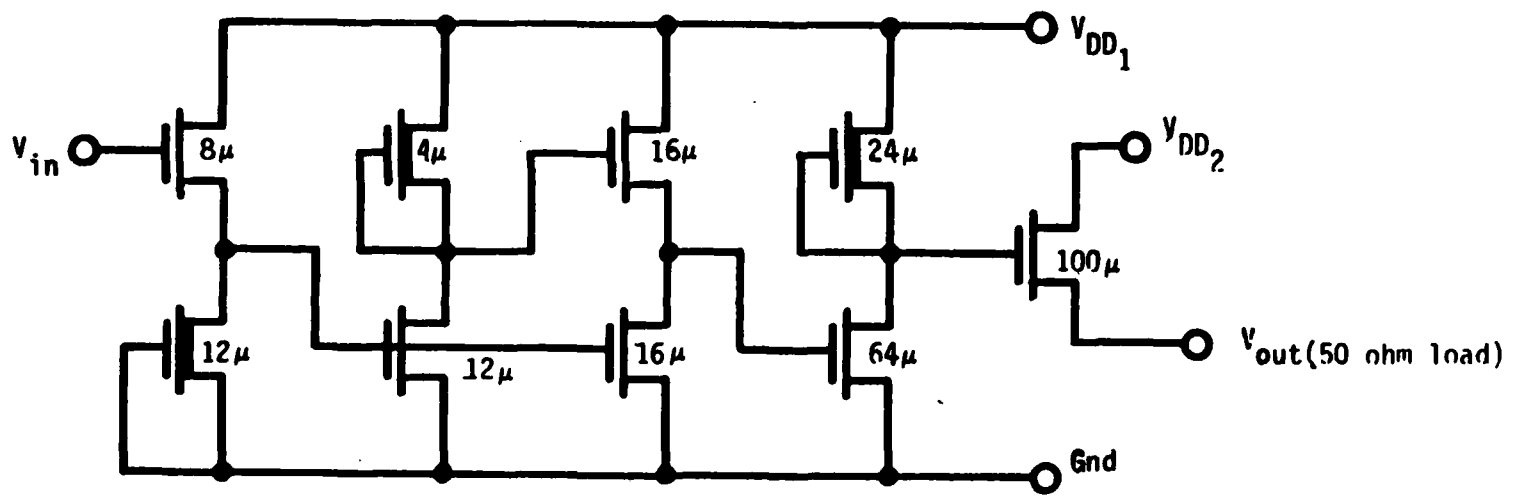

SECTION VII

CIRCUIT LAYOUT

The geometric layout rules were based upon a combination of electrical parameters and achievable line widths using contact printing and wet chemical processing. First, consideration was given to the minimum source drain spacing for the InP MIS transistors. Large spacings are easy to produce, but result in lower gain, higher capacitance devices. As the spacing is reduced the devices exhibit better electrical characteristics but processing becomes difficult and electrical punchthrough between source and drain becomes the limiting factor. Based on past experience in fabrication of InP MISFET devices, a source to drain spacing of 1.5 microns was selected.

Second, the minimum gate width of 4.0 microns was chosen for the InP transistors. Here the compromises were between one of produceabilty, speed, and power. If the devices were selected for low power, say with a 2.0 micron minimum dimension, then processing ease and speed were sacrificed. In the case of speed, stray capacitances of the circuit begin to dominate as transistor sizes shrink. On the other hand if the minimum gate width was selected at 10 microns, then circuit powers begin to climb to unrealistic values. Therefore, the minimum gate width was selected at 4.0 microns.

An additional constraint on the circuit layout was to be able to fabricate the 3x3 multiplier with either an overlapping gate process or as the techniques are developed, a self aligning gate process. The processes are different in that in the overlapping gate process, the gate metal is applied prior to ohmic metallization and in the self aligned gate process, the gate metal is added after ohmic metal is applied. This capability for

interchange of processes was easily accomplished in the multiplier layout without additional masking layers being designed. The primary design consideration was to not place the ohmic metal layer on top of or under the gate metal. The two metal layers were placed side by side in the transistor layout. When it was necessary to connect the two layers, the top layer metallization and a contact via through the interlayer dielectric to the underlying ohmic and gate metals were used. This approach was workable regardless of which process was being utilized.

A list of the geometric design rules used in layout of the various InP circuits is tabulated in Table I. Using these rules for the OR/NAND gate previously described, a complete layout of this circuit is plotted in Figure 15. The most complex building block, the full adder, is shown plotted in detail in Figure 16.

TABLE I

InP DESIGN RULES

DESIGN CONSIDERATION	SPECIFICATION
Source to Drain Spacing	1.5 microns
Minimum Channel Width	4.0 microns
N+ Overlap of Channel	0.5 microns
Gate Metal Width	2.5 microns
Gate Metal Separation	3.0 microns
Gate Metal Overlap of Source/Drain	0.5 microns
Gate Metal Extension Beyound Channel	2.0 microns
Ohmic Metal Width	3.0 microns
Ohmic Metal Extension Beyound Channel	1.0 microns
Top Metal Width	5.0 microns
Top Metal Separation	4.0 microns
Minimum Contact Size	3.0 x 4.0 microns
Top Metal Overlap of Contact	0.5 microns
Bottom Metal to Contact Edge	0.5 microns
Transistor Separation	4.0 microns

Figure 15

INP MULTIPLIER OR/NAND GATE LAYOUT

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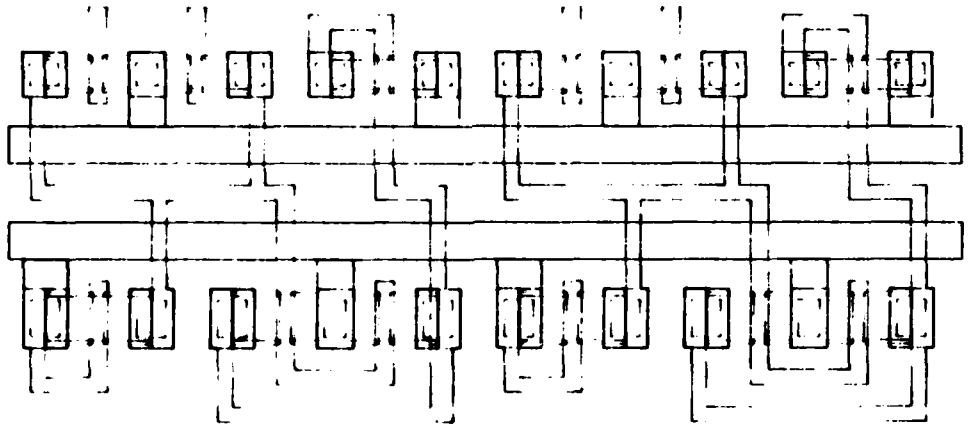

InP MISFET – 3x3 MULTIPLIER

FULL ADDER LAYOUT

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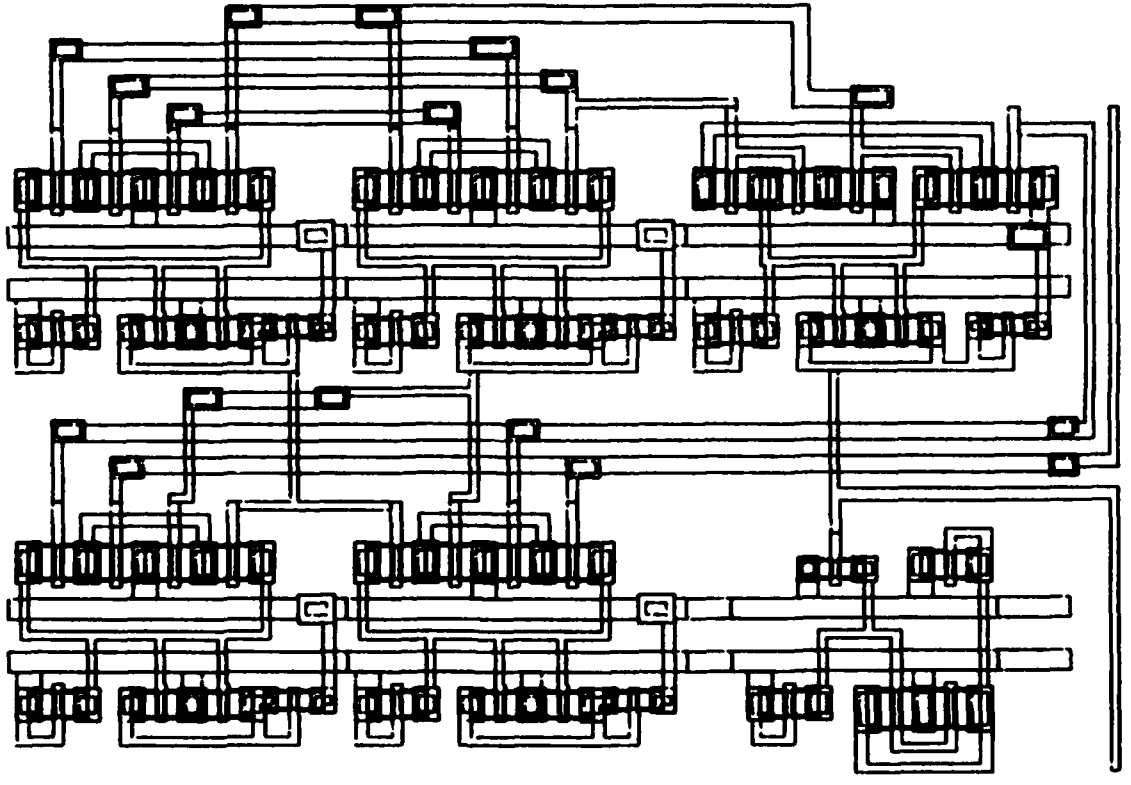
Figure 16



SECTION VIII

CIRCUIT FABRICATION

The step-by-step process for fabrication of the InP MISFET 3x3 multiplier is illustrated in Figure 17. Wafers used for the multiplier were purchased from two souces, Crystalcom and Metals Specialty. The (100) oriented, semi-insulating, iron-doped, 16-17 mil thick wafers were supplied chemically polished on one side. Wafer diameters ranged from 0.75 inches to almost 1.50 inches. The resistiviy was specified to be greator than $5x10^{6}$ ohm-cm. Dislocation density was less than $2x10^{4}$ per cm^{2}.

Fabrication of the multiplier circuit begins with an ultrasonic assisted cleaning operation in a series of solvents. Following an oxygen plasma clean, a photomasking step defines the channel region for the depletion transistor. A light etch using Iodic acid etches the InP to a depth of about 3000 Angstroms thus providing a pattern for alignment of the next mask layers. Following an ion implantation of silicon ions at 65 KEV with doses in the 2.2 to 2.4 $x10^{12}$ range, the photoresist is removed in an oxygen plasma. An optional field implant mask for implanting beryllium into the field regions was available. This mask was never used because leakage currents between actual fabricated devices was not found to be a problem. Another masking step defines the source and drain regions for both the depletion and enhancement (or accumulation) transistors. A second silicon implantation at energies between 60 and 120 KEV and with doses ranging from 5 $x10^{13}$ to 2 $x10^{14}$ provides an N+ layer for low resistance ohmic contacts to the source and drain regions of the InP transistors. Following photoresist removal plus a solvent and acid preclean, both implants are annealed simultaneously at temperatures between 675 ^{o}C and 725 ^{o}C by one of several methods. These include capless techniques such as performed by NOSC or a silicon dioxide cap utilized at Lockheed.

Following ion implant annealling, a photomasking operation defines the regions for ohmic metal contacts to the source and drain regions. Etching of the capping oxide (or else a new layer of oxide for capless annealed wafers) is performed next. This etched oxide layer under the photoresist allows for easy metal liftoff following metal evaporation and is called dielectric assisted metal liftoff. The evaporated metals for ohmic contacts consist of a eutectic composition of a gold-germanium alloy followed by a nickel or platinum layer to maximize wetting of the gold-germanium to the InP surface. Alloying of the metal with the InP is performed at 475 ^{o}C for 20 seconds.

Following complete removal of the capping oxide in buffered HF and a solvent-acid preclean, the gate dielectric of 80-100 nm is deposited by either thermal or indirect plasma-enhanced CVD, the latter oxide being deposted by NOSC. The aluminum gate metal is evaporated to a thickness of 200 nm. Photomasking defines the gate pattern and the aluminum is wet chemically etched. After resist removal a second dielectric layer of SiO_2 is deposited in which vias are etched for contact to the lower levels of metals. The second level of metal interrconnect which is 600 nm of aluminum is evaporated, photomasked and etched. Fabrication of the InP multiplier circuits is completed with a final photoresist strip in an oxygen plasma.

A photomicrograph of the completed InP MISFET 3x3 multiplier is shown in Figure 18. The overall die size of 53 by 67 mils includes the multiplier as well as a row of test structures. The test devices in this row include transistors, sheet resistance monitors, a contact resistance monitor, and a 13 stage ring oscillator using the logic gate of Figure 4c.

InP MISFET MULTIPLIER PROCESS FLOW

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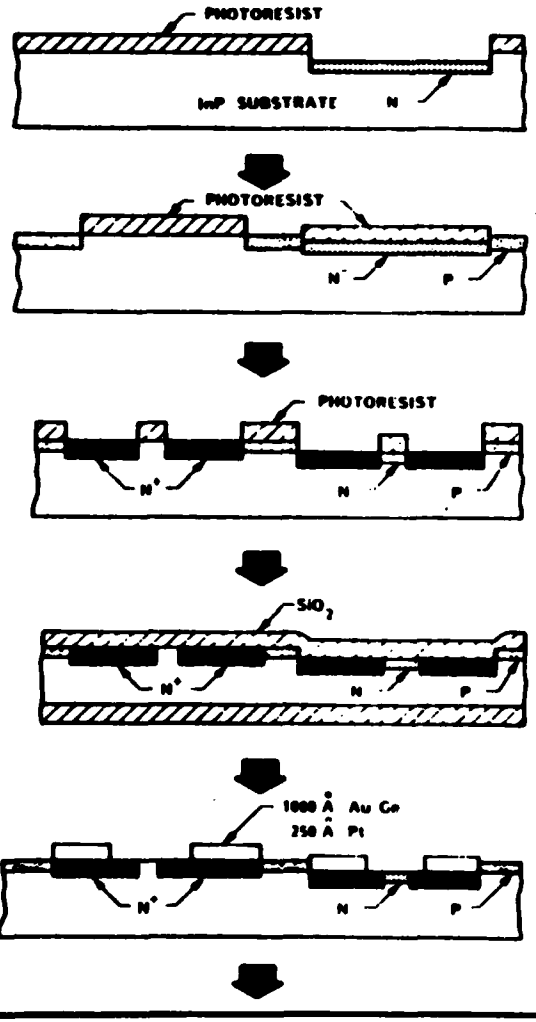
Figure 17



- DEPLETION MASK
- InP ETCH
- N IMPLANT
  - ^{29}Si
  - 60 KEV
  - 1 TO 2 x $10^{12}/cm^2$

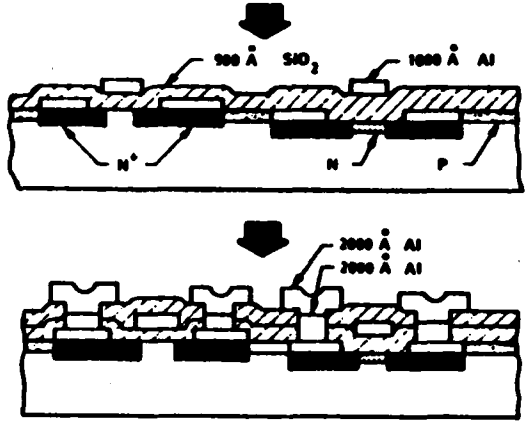
OPTIONAL

- FIELD MASK
- P IMPLANT
  - Be
  - $1 \times 10^{13}/cm^2$

- SOURCE-DRAIN MASK
- N^+ IMPLANT
  - ^{29}Si
  - 60 KEV
  - $5 \times 10^{13}/cm^2$

- SiO_2 CAP
  - FRONT/BACK
  - PHOSPHOROUS DOPED
- ANNEAL
  - 715 TO 725°C
  - 10 MIN IN N_2

- OHMIC METAL MASK
  - Au Ge/Pt LIFT OFF
- ALLOY
  - FORMING GAS
  - 475°C
  - 20 SEC



- GATE DEPOSITION
  - 200°C
  - CVD SiO_2
  - 900 Å
- GATE MASK
  - 1000 Å ALUMINUM

- SiO_2 DEPOSITION
  - 2000 Å
- CONTACT MASK
  - SiO_2 ETCH
  - 2000 Å ALUMINUM

- METAL MASK
  - 2000 Å ALUMINUM

Figure 18

InP 3x3 MULTIPLIER DIE PHOTO

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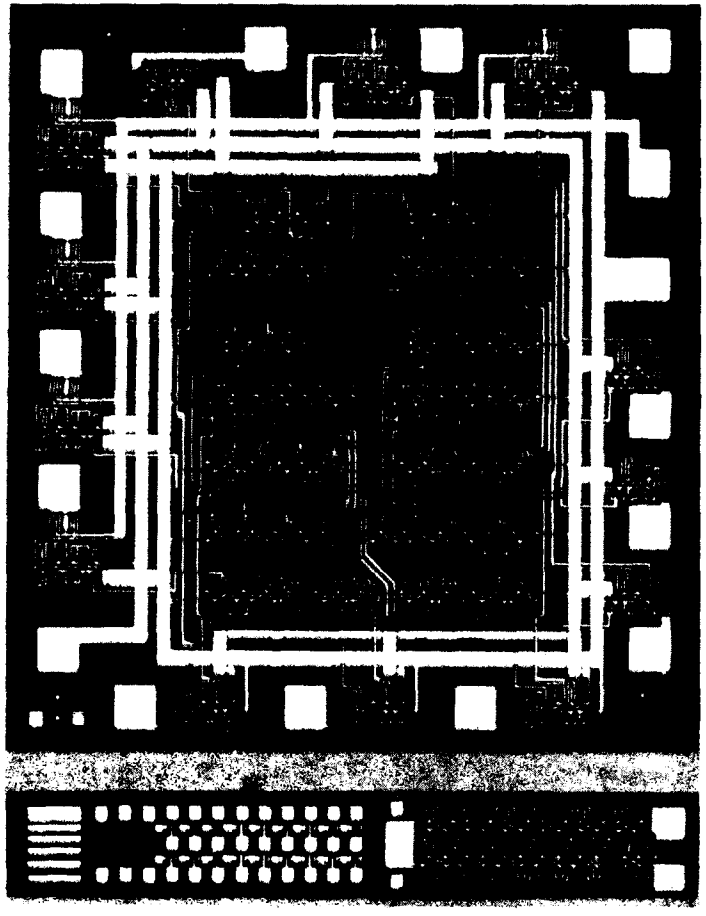

SECTION IX

TEST RESULTS

The InP MISFET 3x3 multiplier has been tested and found to be partially functional with many of the subcircuits operational. Complete multiplier operation would have been possible had a mask error not existed. This mask error left a portion of the multiplier without any signals from previous adder circuits when certain input combinations were applied. With this circuit layout condition, only three of the output product bits, P0 through P2, functioned under all combinations of input signals. Even with this mask error the multiplier was able to function in the self test mode.

Shown in Figure 19 are curve tracer photos revealing current-voltage characteristics of InP MISFET devices. The transistors are 10 microns wide with a 1.5 micron source drain spacing. The depletion device drain current characteristics are shown with its gate connected to its source as this is the mode in which these devices were operated in the multiplier. The enhancement (accumulation) device is shown with gate voltage steps ranging from 0 to 7.0 volts. From the photo of Figure 19, the turn on voltage is approximately 0.5 volts. This positive turn on voltage insures that the logic gates will operate with good noise margins. Transconductances for these devices are between 25 and 35 ms/mm, about one half to one third the expected amount. We found no particular reason for this low value execpt that material and process variations have produced similar results in the past. The 10 x 1.5 micron size depletion transistors when used as constant current sources, as shown in Figure 19, operated with a saturated current of approximately 0.5 ma.

Using the logic gate of Figure 4c, a 13 stage ring oscillator was included in the test row as previously mentioned. These ring oscillators were found to yield as high as 50 percent in functionality on several wafers. This is a strong indication of the increasing maturity of the InP MISFET technology. A typical oscillator output waveform for an oscillator is shown Figure 20.

Figure 19

INP MISFET

TRANSISTOR CHARACTERISTICS

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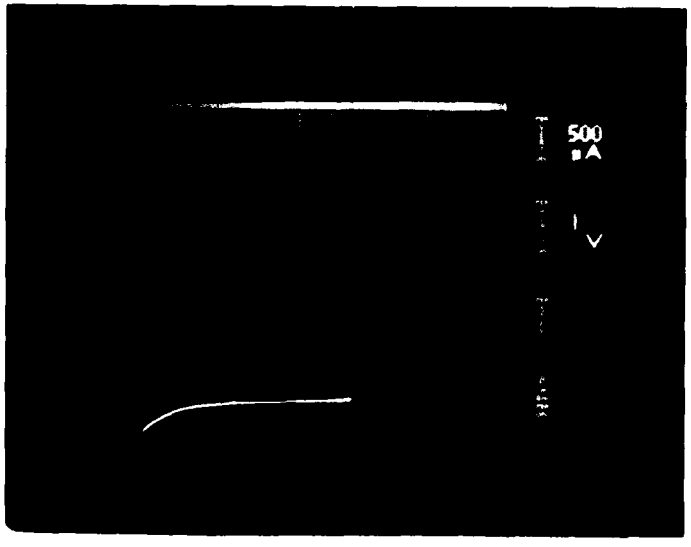
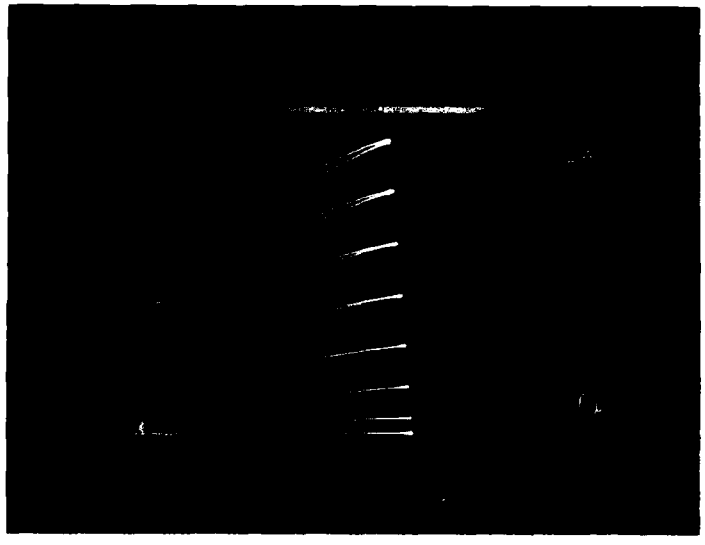


10 x 1.5 Micron
Depletion Device
(Gate Connected To Source)



10 x 1.5 Micron
Enhancement Device

Figure 20

InP RING OSCILLATOR RESULTS

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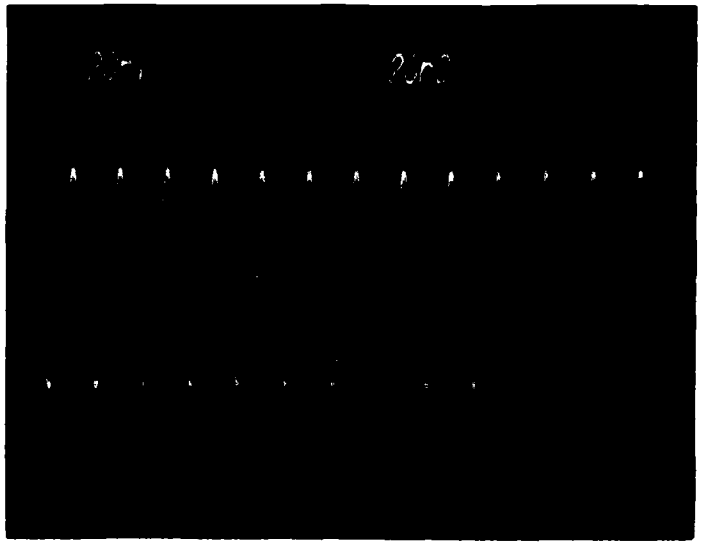

13 STAGE RING OSCILLATOR

T_p = 500 ps

The propagation delay for an inverter can be calculated from the period of oscillation of the ring oscillator as follows:

$$t_{pd} = \frac{\text{Period of oscillation}}{2 \times \text{number of stages}}$$

For this design the best best t_{pd} was 500 ps. This switching delay was approximately a factor of two to three higher than expected but when considering the low transconductances of the devices, this result is appropriate.

Individual logic functions used in the multiplier were tested by direct probing on the wafer with finely adjusted probes. Input signals were applied directly to the logic gates without use of input buffers. Logic gate outputs were also measured directly on chip. This way logic and circuit design verification was possible without a separate chip design in which these circuits would be isolated. Furthermore by direct probing, an input signal can be followed through the various logic elements. This technique helps to isolate mask layout errors.

The operation of the OR/NAND gate of Figure 9 was characterized by this method of direct on-chip testing. Shown in Figure 21 are low frequency signals applied to and also measured on an InP OR/NAND gate. The square wave signal depicted at the top of the photo is applied to the upper pair of transistors. When a pulsed signal is supsequently applied to the the middle pair of transistors, the output of the OR/NAND gate changes. This waveform verifies the logic of this gate in that two positive signals are required on the series input transistors before a low voltage is observed on the output.

A more complicated gate which was characterized directly on the multiplier is the Full Adder circuit of Figure 12. A waveform was applied to the adder circuit such that various combinations of X, Y and C-in could be examined. The photo of Figure 22 shows such a combination of input conditions.

The experimental results of the Full Adder circuit can be explained with help from the logic truth table below.

X	Y	C-in	C-out
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	0
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	0

From the above truth table for a full adder, a logic zero occurs at the C-out node whenever any two input combinations are a logic one. Some of these test conditions are created in the photo of Figure 22. The top square wave signal represents the X input to the Full Adder circuit. The next two waveforms, which are short positive pulses, represent the Y and C-in signals respectively. The bottom signal is the C-out waveform for the adder circuit. This input waveform timing configuration results in two output pulses from the adder. A timing cycle starts with a positive voltage applied to the X input of the Full Adder. From the output waveform photo a slightly negative step occurs as a result of some capacitive coupling. The next positive pulse, which is relatively short compared to the X input, is the C-in signal. From the above truth table, when X and C-in are both logic one, the output is required to be logic zero. As observed in the output waveform photo, this requirement is correctly performed. Next, the C-in signal is switched low and the C-out signal returns to logic one. A short time later, another pulse is applied to the Full Adder circuit. This time the signal is the Y input. Again the output responds in the correct manner. The cycle ends with the X input returning to zero. These sequences of pulses applied to the Full Adder circuit demonstrate the correct operation of the Full Adder design for the 3x3 multiplier.

Figure 21

INP OR/NAND GATE

OPERATIONAL CHARACTERISTICS

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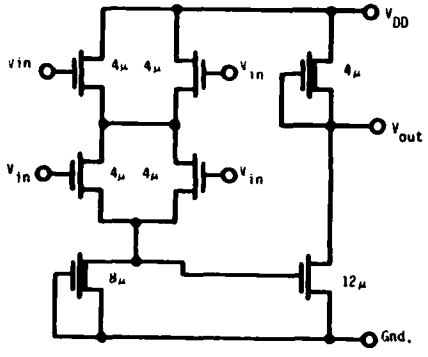

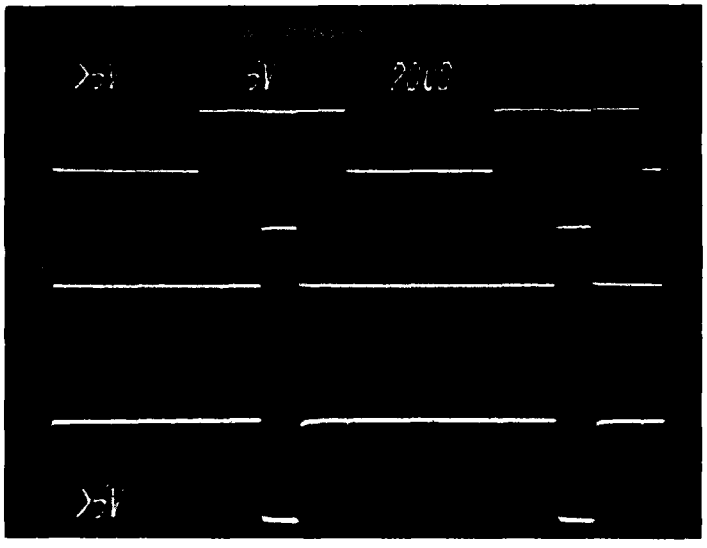

Figure 22

INP FULL ADDER

OPERATIONAL CHARACTERISTICS

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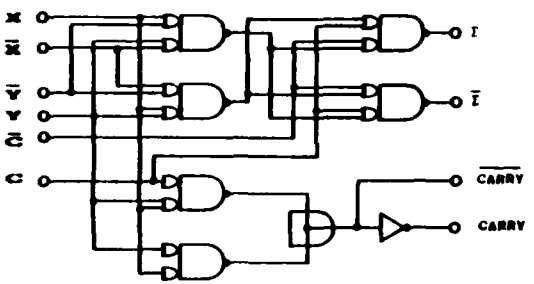

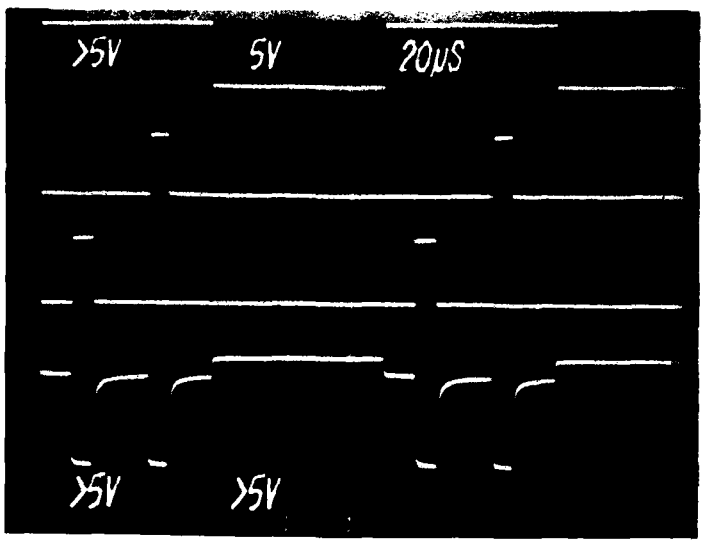

Final testing of the multiplier involves the self-test or ring oscillator mode of the mulitplier. The best results achieved for this test were 11 ns. To achieve oscillation in the multiplier, the most significant data bit is logically inverted and applied to the least significant input bit. In this mode the multiplier exercises the longest time delay path and this is an indicator of longest muliplication times. Also the greatest number of logic gates are used for this test. Shown in Figure 23 are the waveforms resulting from this test. The sequence starts with a positive signal being applied to all the Y inputs and to the X3 input of the multiplier. This meets part of the criteria for self oscillation as shown in the equation of Figure 3. As a result of this signal, the output at the most significant bit of the multiplier switches to a high state. A short time later, another signal is applied, this time to the self test control input, which results in bit P5 being inverted and directed to the X0 input as shown in Figure 3. The multiplier now is able to oscillate as the photo of Figure 23 shows. An expanded time scale representation of the oscillation signal is at the bottom of the photo which illustrates the wave shape of the multiplier output in the ring oscillator mode. Measured multiply times of 11 ns were over three times the expected results which are a result of lower than expectecd transistor transconducatances. On the positive side these results did demonstrate that a large number of working InP logic gates were found functional in the 3x3 multiplier.

InP 3x3 MULTIPLIER SELF TEST MODE

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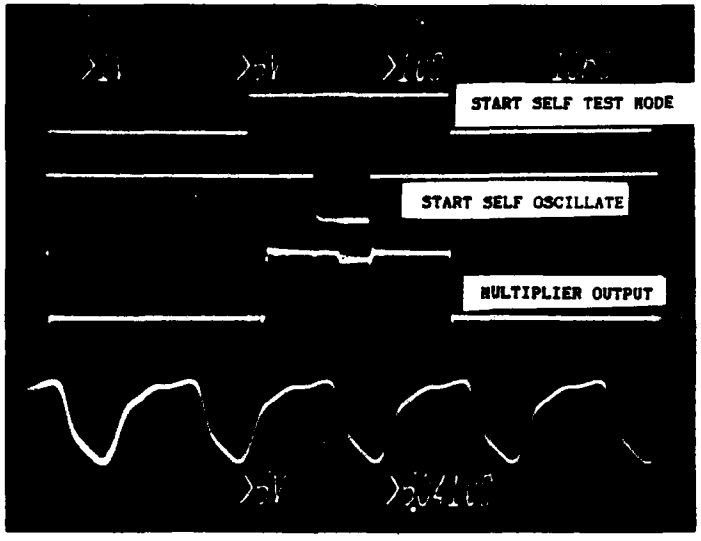

Figure 23

InP 3x3 MULTIPLIER - SELF TEST
11 ns MULTIPLY TIME

SECTION X

SUMMARY AND CONCLUSIONS

A 3x3 digital multiplier integrated circuit has been developed using InP MISFET technology. The architectural design of the 3 x 3 multiplier uses three full adder and three half adder circuits for the addition process and two-input nor gates for bit multiplication. A modified enhancement/depletion circuit approach with source follower input transistors results in process tolerant noise immunities. The channel lengths of the InP transistors are 1.5 microns with 4 microns being the minimum channel width. The multiplier fabrication process uses selective ion implantaion into semi-insulated InP wafers for forming the active devices. The process uses silicon dioxide for the gate dielectric and aluminum for dual layer metallization. Transistors fabricated with this approach exhibited maximum transconductances of 35 ms/mm. InP logic gates designed into a special test row of the multiplier in the form of a 13 stage ring oscillator resulted in propagation delays of 500 ps per inverter. All of the individual logic blocks were found functional for fabricated multiplier circuits, although a mask layout error prevented testing of fully operational circuits. In a self test mode in which the multiplier is operated as a ring oscillator, multiply times of 11 ns were observed.

This technology is at a point of maturity where approximately a hundred logic gates can be integrated for a design. Yields of InP MISFET devices fabricated in class 100 to class 1000 clean room environments are adequate to produce circuits of this complexity. Two continuing areas of development are needed to further enhance this technology. First of all, material development is needed in order to control background impurities which affect device thresholds from wafer to wafer. More control of threshold voltages will result in simplier circuit implementation of logic gates. Secondly, an improved dielectric is needed which consistantly results in devices with high transconductances. This effort will result in InP circuits that operate with the full promise of this technology.

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